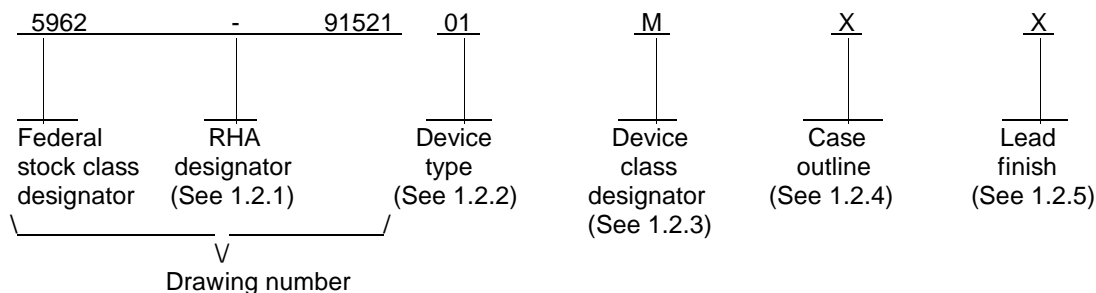


NOTICE OF REVISION (NOR) (See MIL-STD-480 for instructions) This revision described below has been authorized for the document listed.		DATE (YYMMDD) 94-08-12	Form Approved OMB No. 0704-0188							
Public reporting burden for this collection is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Information and Regulatory Affairs, Office of Management and Budget, Washington, DC 20503.										
1. ORIGINATOR NAME AND ADDRESS Defense Electronics Supply Center 1507 Wilmington Pike Dayton, Ohio 45444-5277		2. CAGE CODE 67268	3. NOR NO. 5962-R230-94							
		4. CAGE CODE 67268	5. DOCUMENT NO. 5962-91521							
6. TITLE OF DOCUMENT MICROCIRCUIT, LINEAR, 12-BIT DATA ACQUISITION SYSTEM, 4-CHANNEL SIMULTANEOUS SAMPLING, MONOLITHIC SILICON		7. REVISION LETTER (Current)	(New) A							
		8. ECP NO. No registered users								
9. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES All										
10. DESCRIPTION OF REVISION Sheet 1: Revisions ltr column; add "A" Revisions description column; add "Changes in accordance with NOR 5962-R230-94". Revisions date column; add "94-08-12" Revisions level block; add "A". Rev status of sheets; For sheets 1, 7, 8, and 9, add "A". Sheet 7: Table I. ANALOG INPUTS section, add footnote "6/". REFERENCE OUTPUT section, delete footnote "6/". Rev level block; add "A". Sheet 8 Table I. Logic input current test. Delete and substitute the following: <table border="1" style="width: 100%; border-collapse: collapse; margin: 10px 0;"> <tr> <td style="padding: 5px;">Logic input current</td> <td style="padding: 5px;">I_{IN}</td> <td style="padding: 5px;">V_{IN} 0 V to V_{DD} $V_{DD} = +5.25$ V, $V_{SS} = -5.25$ V</td> <td style="padding: 5px;">1,2,3</td> <td style="padding: 5px;"></td> <td style="padding: 5px;">± 10</td> <td style="padding: 5px;">μA</td> </tr> </table> Sheet 9: TABLE I. Data access time after \overline{RD} test. Under the limits column, delete "70 ns minimum" and substitute "70 ns Maximum". Revision level block; add "A".				Logic input current	I_{IN}	V_{IN} 0 V to V_{DD} $V_{DD} = +5.25$ V, $V_{SS} = -5.25$ V	1,2,3		± 10	μA
Logic input current	I_{IN}	V_{IN} 0 V to V_{DD} $V_{DD} = +5.25$ V, $V_{SS} = -5.25$ V	1,2,3		± 10	μA				
11. THIS SECTION FOR GOVERNMENT USE ONLY										
a. CHECK ONE <input checked="" type="checkbox"/> EXISTING DOCUMENT SUPPLEMENTED <input type="checkbox"/> REVISED DOCUMENT MUST BE <input type="checkbox"/> CUSTODIAN OF MASTER DOCUMENT BY THIS NOR MAY BE USED IN RECEIVED BEFORE MANUFACTURER SHALL MAKE ABOVE REVISION AND MANUFACTURE. MAY INCORPORATE THIS CHANGE. FURNISH REVISED DOCUMENT TO:										
b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT DESC-ELDS	SIGNATURE AND TITLE MICHAEL A. FRYE Chief, Custom Microelectronics		DATE (YYMMDD) 94-08-12							
12. ACTIVITY ACCOMPLISHING REVISION DESC-ELDS	REVISION COMPLETED (Signature) RICK C. OFFICER		DATE (YYMMDD) 94-08-12							

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	AD7874	12-bit data acquisition system, 4-channel simultaneous sampling

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
---------------------	--

M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
---	---

B or S	Certification and qualification to MIL-M-38510
--------	--

Q or V	Certification and qualification to MIL-I-38535
--------	--

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

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1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Positive supply voltage range (V_{DD}) to AGND -----	-0.3 V dc to +7.0 V dc
Positive supply voltage range (V_{DD}) to DGND -----	-0.3 V dc to +7.0 V dc
Negative supply voltage range (V_{SS}) to AGND -----	+0.3 V dc to -7.0 V dc
AGND to DGND -----	-0.3 V dc to $V_{DD} + 0.3$ V dc
Analog input range (V_{IN}) -----	-15.0 V dc to + 15.0 V dc
Voltage reference output (REF OUT) to analog ground range (AGND) -----	0 V dc to V_{DD}
Logic input voltage range -----	-0.3 V dc to $V_{DD} + 0.3$ V dc
Logic output voltage range -----	-0.3 V dc to $V_{DD} + 0.3$ V dc
Thermal resistance, junction-to-case (Θ_{JC})-----	See MIL-STD-1835
Maximum power dissipation (P_D) 2/ -----	1,000 mW
Lead temperature (soldering, 10 sec.) -----	+300° C
Storage temperature range -----	-65° C to +150° C

1.4 Recommended operating conditions.

Positive supply voltage range (V_{DD}) -----	+4.75 V dc to +5.25 V dc
Negative supply voltage range (V_{SS}) -----	-4.75 V dc to -5.25 V dc
Analog input voltage range -----	-10.0 V dc to +10.0 V dc
Ambient operating temperature range (T_A)-----	-55° C to +125° C
Reference input voltage range -----	+2.85 V dc to +3.15 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510	-	Microcircuits, General Specification for.
MIL-I-38535	-	Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480	-	Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883	-	Test Methods and Procedures for Microelectronics.
MIL-STD-1835	-	Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Above $T_A = +75^\circ\text{C}$, derate at a factor of 10 mW/° C for X package, and above $T_A = +66^\circ\text{C}$, derate at a factor of 10 mW/° C for 3 package.

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BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block or logic diagram. The block or logic diagram shall be as specified on figure 2.

3.2.4 Timing diagram. The timing diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

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3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 93 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55° C ≤ T _A ≤ +125° C +4.75 V ≤ V _{DD} ≤ +5.25 V -5.25 V ≤ V _{SS} ≤ -4.75 V unless otherwise specified	Group A subgroups	Limits 2/		Units
				Min	Max	
SAMPLE AND HOLD						
Acquisition time to 0.01 pct	t _{ACQ}	3/ 4/ See figure 3	9,10,11		2.0	μs
Aperture delay	t _{AU}		9,10,11	0	40	ns
Aperture delay matching	ADM				4.0	
SAMPLE AND HOLD AND ADC DYNAMIC PERFORMANCE						
Signal-to-noise ratio	SNR	f _{IN} = 10 kHz sine wave, f _{sample} = 29 kHz	1,2,3	70		dB
Total harmonic distortion	THD				-78	
Peak harmonic	PH					
Intermodulation distortion		f _a = 9 kHz, f _b = 9.5 kHz, f _{sample} = 29 kHz				
2nd order terms 3rd order terms	IMD2 IMD3					
Channel-to-channel isolation	ISO					
DC ACCURACY						
Relative accuracy	INL	4/	1,2,3		±1	LSB
Differential nonlinearity	DNL	4/ No missing codes guaranteed				

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ $+4.75\text{ V} \leq V_{DD} \leq +5.25\text{ V}$ $-5.25\text{ V} \leq V_{SS} \leq -4.75\text{ V}$ unless otherwise specified	Group A subgroups	2/ Limits		Units
				Min	Max	
Positive 5/ full-scale error	PFSE	Any channel	1,2,3		± 5	LSB
Negative 5/ full-scale error	NFSE					
Full-scale error match	FSEM	Between channels			5	
Bipolar zero error	BZE	Any channel			± 5	
Bipolar zero error match	BZEM	Between channels			4	

ANALOG INPUTS

Analog input current	AIN		1,2,3		± 600	μA
----------------------	-----	--	-------	--	-----------	---------------

REFERENCE OUTPUT 6/ $V_{DD} = +5\text{ V}$, $V_{SS} = -5\text{ V}$

Reference output voltage error	ROVE		1		± 0.33	%
			2,3		± 1.0	
Reference output load change	ROLC	Reference load current change (0-500 microamps)	1,2,3		± 2.0	mV

REFERENCE INPUT

Reference input current	RIC	$V_{REF} = +3\text{ V}$	1,2,3		± 1.0	μA
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See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	1/ Conditions $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ $+4.75\text{ V} \leq V_{DD} \leq +5.25\text{ V}$ $-5.25\text{ V} \leq V_{SS} \leq -4.75\text{ V}$ unless otherwise specified	Group A subgroups	2/ Limits		Units
				Min	Max	
Reference input capacitance	C_{REF}	$T_A = +25^{\circ}\text{C}$	4		10	pF
LOGIC INPUTS						
High level logic input voltage	V_{INH}	\underline{Z}	7, 8	2.4		V
Low level logic input voltage	V_{INL}	\underline{Z}			0.8	
Logic input current	I_{IN}	$V_{IN} = 0\text{ V to } V_{DD}$ $V_{DD} = +5.2\text{ V}, V_{SS} = -5.2\text{ V}$	1,2,3		± 10	μA
Logic input capacitance	C_{IN}	$T_A = +25^{\circ}\text{C}$	4		10	pF
LOGIC OUTPUTS						
High level logic output voltage	V_{OH}		1,2,3	4.0		V
Low level logic output voltage	V_{OL}				0.4	
Logic output floating-state leakage current	LOFSLC	$V_{IN} = 0\text{ V to } V_{DD}$ DB0 - DB11 $V_{DD} = +5.25\text{ V}, V_{SS} = -5.25\text{ V}$			± 10	μA
Logic output floating-state output capacitance	C_{OUT}	$T_A = +25^{\circ}\text{C}$	4		10	pF
POWER REQUIREMENTS $V_{DD} = +5.25\text{ V}, V_{SS} = -5.25\text{ V}$						
Positive supply current	I_{DD}	$CS = RD = CONVST = +5.0\text{ V}$	1,2,3		18	mA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C +4.75 V ≤ V _{DD} ≤ +5.25 V -5.25 V ≤ V _{SS} ≤ -4.75 V unless otherwise specified	Group A subgroups	Limits		Units
				Min	Max	
Negative supply current	I _{SS}	CS = RD = CONVST = +5.0 V	1,2,3		12	mA
Power dissipation	P _D	V _{DD} = 5 V, V _{SS} = -5 V			150	mW
AC CHARACTERISTICS						
8/						
CONVST pulse width	t ₁	T _A = +25°C, See figure 3 9/	9	50		ns
CS to RD setup	t ₂	T _A = +25°C, See figure 3 9/		0		
RD pulse width	t ₃	See figure 3	9,10,11	70		
CS to RD hold	t ₄	T _A = +25°C, See figure 3 9/	9	0		
RD to INT delay	t ₅	T _A = +25°C, See figure 3 9/			60	
Data access time after RD	t ₆	See figure 3 10/	9,10,11	70		
Bus relinquish time after RD	t ₇	See figure 3 11/		5	50	
Delay time between reads	t ₈	T _A = +25°C, See figure 3 9/	9	150		
CONVST to INT, external clock = 2.5 MHZ	t _{CONV}	T _A = +25°C, See figure 3 9/	9	31.0	32.5	μs
CONVST to INT, internal clock	t _{CONV}	T _A = +25°C, See figure 3 9/		31.0	35.0	
Minimum input clock period	t _{CLK}	T _A = +25°C 9/			10	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued

- 1/ $V_{REF} = +3\text{ V}$, $AGND = DGND = 0\text{ V}$. All tests are guaranteed over a supply voltage range of $V_{DD} = +5\text{ V} \pm 5\%$, $V_{SS} = -5\text{ V} \pm 5\%$; however, all measurements are made at $V_{DD} = +4.75\text{ V}$, $V_{SS} = -4.75\text{ V}$ unless otherwise specified.
- 2/ The limiting terms "min" (minimum) and "max" (maximum) shall be considered to apply to magnitudes only. Negative current shall be defined as conventional current flow out of a device terminal.
- 3/ S/H acquisition time is tested by performing an FFT test using an acquisition time equal to the test limit value. This same test is used to determine SNR and THD. Acquisition time is guaranteed by an SNR value which meets the test limit for that specification.
- 4/ Tested on one channel only. The channel used for testing is that which shows the worst performance in device characterization.
- 5/ Measured with respect to the REF IN voltage and includes bipolar offset error.
- 6/ For capacitive loads greater than 50 pF, a series resistor is required.
- 7/ These tests are performed by using the test limits as setup conditions. Part functionality guarantees that the tested parameters meet specification.
- 8/ All input signals are specified with $t_r = t_f = 5\text{ ns}$ (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
- 9/ Measured only for initial qualification and after any process or design changes which may affect these parameters.
- 10/ t_6 is measured with the load circuit of figure 4 and defined as the time required for an output to cross 0.8 V or 2.4 V.
- 11/ t_7 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of figure 5. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_7 , quoted in the timing characteristics, is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

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Device type	01
Case outlines	X and 3
Terminal number	Terminal symbol
1	V_{IN1}
2	V_{IN2}
3	V_{DD}
4	INT
5	CONVST
6	RD
7	CS
8	CLK
9	V_{DD}
10	DB11
11	DB10
12	DB9
13	DB8
14	DGND
15	DB7
16	DB6
17	DB5
18	DB4
19	DB3
20	DB2
21	DB1
22	DB0
23	AGND
24	REF IN
25	REF OUT
26	V_{SS}
27	V_{IN3}
28	V_{IN4}

FIGURE 1. Terminal connections.

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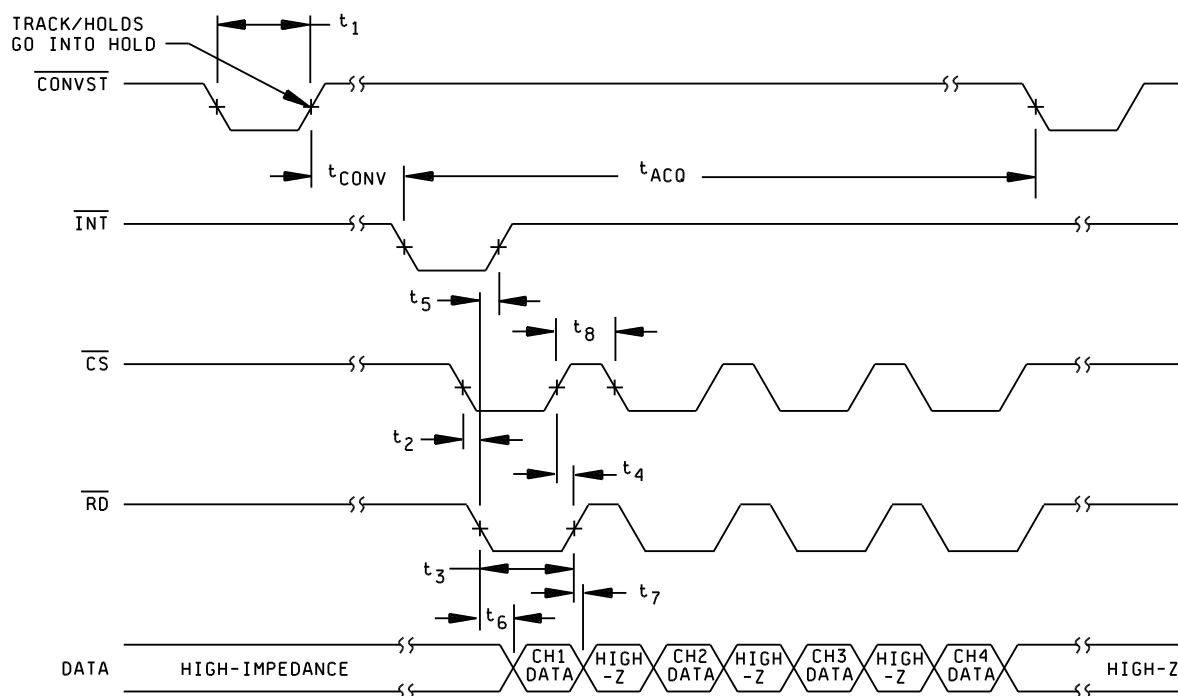


FIGURE 3. Timing diagram.

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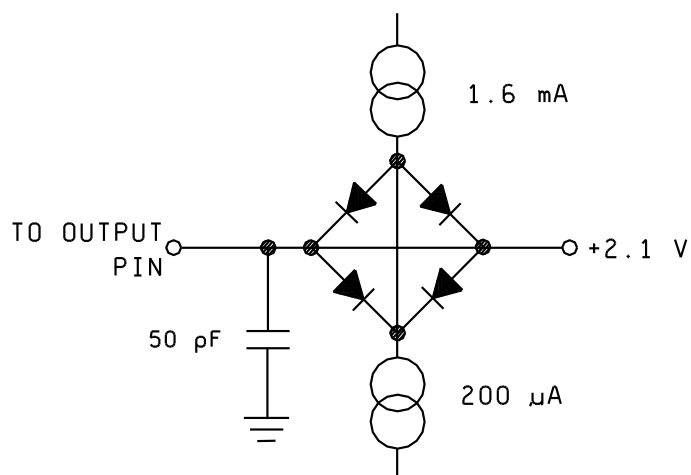


FIGURE 4. Load circuit access time.

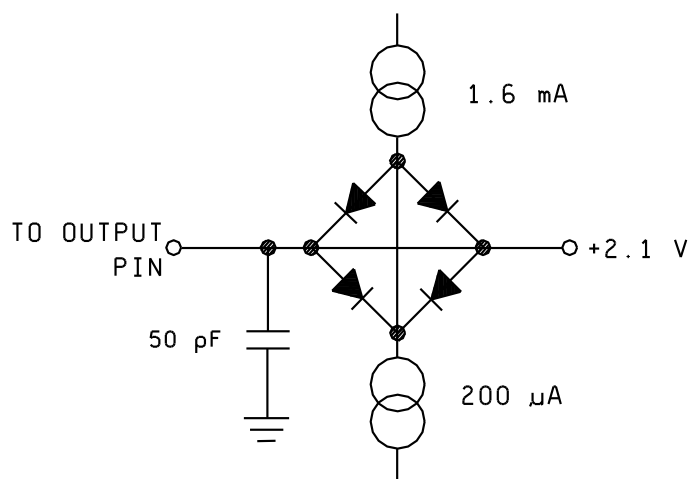


FIGURE 5. Load circuit for bus relinquish time.

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4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_{IN} , C_{REF} , and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition B or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1	1	---
Final electrical parameters (see 4.2)	1/ 1,2,3, 7,8	1/ 1,2,3, 7,8	1/ 1,2,3, 7,8	1/ 1,2,3, 7,8	1/ 1,2,3, 7,8
Group A test requirements (see 4.4)	1,2,3 4,7,8, 9,10,11	1,2,3, 4,7,8, 9,10,11	1,2,3, 4,7,8, 9,10,11	1,2,3, 4,7,8, 9,10,11	1,2,3, 4,7,8, 9,10,11
Group B end-point electrical parameters (see 4.4)	---	---	1,2,3	---	---
Group C end-point electrical parameters (see 4.4)	1	1	---	1	1,2,3
Group D end-point electrical parameters (see 4.4)	1	1	1	1	1
Group E end-point electrical parameters (see 4.4)	1	1	1	1	1

1/ PDA applies to subgroup 1.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

- End-point electrical parameters shall be as specified in table II herein.
- For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$, after exposure, to the subgroups specified in table II herein.
- When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

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6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document listing</u>
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY (Part 1 or 2)	QPL-38510	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 92-11-30

Approved sources of supply for SMD 5962-91521 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN <u>1/</u>
5962-9152101MXX	24355	AD7874SQ/883B
5962-9152101M3X	24355	AD7874SE/883B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

24355

Vendor name
and address

Analog Devices, Incorporated
Route 1 Industrial Park
P.O. Box 9106
Norwood, MA 02062
Point of contact:

804 Woburn Street
Wilmington, MA 01887

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.
